Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **J**
4. **K**
5. **C**
6. **D**
7. **VSS**
8. **E**
9. **F**
10. **L**
11. **M**
12. **G**
13. **H**
14. **VDD**

**1 14 13**

**6 7 8 9**

**2**

**3**

**4**

**5**

**12**

**11**

**10**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .063” X .065” DATE: 8/25/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: CD4070BH**

**DG 10.1.2**

#### Rev B, 7/19/02